

What Is Claimed Is:

1 1. A liquid crystal display panel, driven by a column
2 inversion driving mode, comprising:

3 a plurality of parallel data lines, disposed along an
4 X-axis;

5 a plurality of parallel scan lines, disposed along a
6 Y-axis;

7 a plurality of display unit pixels, each having a control
8 transistor, a storage capacitor, a common electrode,
9 and a pixel electrode, wherein each set of two
10 adjacent data lines and two adjacent scan lines
11 defines the boundary of one display unit pixel
12 wherein each data line interlaces with both scan
13 lines; and

14 a plurality of display unit blocks disposed in array, each
15 having display unit pixels parallel to and disposed
16 sequentially along two adjacent data lines, wherein
17 the display unit pixels within any display unit block
18 between two adjacent data lines are coupled to one
19 of the two adjacent data lines, while the display unit
20 pixels within another adjacent display unit block
21 between the two adjacent data lines are coupled to
22 the other of the two adjacent data lines.

1 2. The liquid crystal display panel as claimed in claim
2 1, wherein the display unit pixels within any display unit block
3 in a row and the display unit pixels within another adjacent
4 display unit block in the row are coupled to different data
5 lines.

1 3. The liquid crystal display panel as claimed in claim
2 1, wherein the common electrode and the pixel electrode make up
3 a liquid capacitor.

1 4. A liquid crystal display panel, driven by a column
2 inversion driving mode, comprising:

3 a plurality of data lines having a first data line and a
4 second data line;

5 a plurality of scan lines having a first scan line and a
6 second scan line;

7 a plurality of display unit pixels, each having a control
8 transistor, a storage capacitor, a common electrode,
9 and a pixel electrode, wherein each set of two
10 adjacent parallel data lines and two adjacent
11 parallel scan lines defines the boundary of one
12 display unit pixel wherein each data line interlaces
13 with both scan lines;

14 a first display unit block disposed between the first and
15 the second data lines and having the display unit
16 pixels parallel to and disposed sequentially along
17 the first and the second data lines, wherein the
18 display unit pixels are coupled to the first data
19 line; and

20 a second display unit block disposed between the first and
21 the second data lines, adjacent to the first display
22 unit block, and having the display unit pixels
23 parallel to and disposed sequentially along the first
24 and the second data lines, wherein the display unit
25 pixels are coupled to the second data line.

1 5. The liquid crystal display panel as claimed in claim
2 4, further comprising:

3 a third data line;

4 a third scan line;

5 a third display unit block disposed between the second and
6 the third data lines and having the display unit
7 pixels parallel to and disposed sequentially along
8 the second and the third data lines, wherein the
9 display unit pixels are coupled to the second data
10 line; and

11 a fourth display unit block disposed between the second and
12 the third data lines, adjacent to the third display
13 unit block, and having the display unit pixels
14 parallel to and disposed sequentially along the
15 second and the third data lines, wherein the display
16 unit pixels are coupled to the third data line.

1 6. The liquid crystal display panel as claimed in claim
2 4, wherein the common electrode and the pixel electrode make up
3 a liquid capacitor.

1 7. The liquid crystal display panel as claimed in claim
2 4, wherein the polarity of the first display unit block is
3 opposite that of the second display unit block upon completion
4 of the column inversion driving mode.

1 8. The liquid crystal display panel as claimed in claim
2 5, wherein the common electrode and the pixel electrode make up
3 a liquid capacitor.

1 9. The liquid crystal display panel as claimed in claim
2 5, wherein upon completion of the column inversion driving mode,
3 the polarity of the first display unit block is the same as that
4 of the fourth display unit block, and polarities of both the
5 second and the third display unit blocks are opposite those of
6 the first display unit block.